REMARKS

Applicant appreciates the thorough examination of the application that is reflected in the Office Action dated September 12, 2002. Claims 1, 5, and 7 are amended; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Independent claims 1 and 7 have been amended to further distinguish over the cited references. Claims 1-19 and 32-31 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Claims 1-6

Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by US PG Pub 2001/0033001 to Kato (hereinafter "Kato") or US Patent Number 6,384,452 to Chittipeddi et al. (hereinafter "Chittipeddi"), and under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,933,715 to Igel et al (hereinafter "Igel").

Claim 1 has been amended. Amended claim 1 relates to a semiconductor device, comprising:

> a semiconductor substrate having a first conductive layer provided therein;
> an insulation layer provided above the semiconductor substrate;
> a semiconductor layer provided above the insulation layer, wherein the semiconductor layer includes an element isolation region which has a connection hole;
> a second conductive layer provided above the semiconductor layer or in the semiconductor layer, and electrically connected to the first conductive layer; and
> a contact layer provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer. (Emphasis added.)

Applicant submits that the cited references fail to teach or suggest all of the recitations of claim 1. The Kato, Chittipeddi, and Igel references all fail to teach or suggest, for example, that "semiconductor layer includes an element isolation region which has a connection hole," and "a contact layer provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer," as required by claim 1. Applicant therefore respectfully submits that claim 1 is patentable over the cited references for at least the foregoing reasons. Applicant further submits that claims 2-6 are patentable at least by virtue of their dependency from claim 1.

Claim 5

Claim 5 depends from claim 1, and is therefore patentable at least by virtue of its dependency from claim 1. In addition, Applicant respectfully submits that the Kato and Igel references fail to teach or suggest recitations of claim 5.

For example, Applicant respectfully submits that Kato and Igel both fail to teach or suggest "the connection hole extends into the semiconductor substrate", as recited in claim 5. Accordingly, the rejection of claim 5 based on Kato and Igel should also be withdrawn.

Claims 7-13

Claim 7 was rejected under 35 U.S.C. 102(e) as being anticipated by Kato or US Patent Number 6,188,122 to Davari et al. (hereinafter "Davari"), and under 35 U.S.C. 102(b) as being anticipated by Igel et al. or US Patent Number 5,879,971 to Witek (hereinafter "Witek").

Claim 7 has been amended. Amended claim 7 relates to a semiconductor device, comprising:

> a semiconductor substrate having a contact region provided therein;
> an insulation layer provided above the semiconductor substrate; and
> a semiconductor layer provided above the insulation layer, wherein the semiconductor layer includes an element isolation region which has a connection hole;
> a conductive layer provided above the semiconductor layer or in the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, the contact region being electrically connected to the conductive layer; and
> a contact layer provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer. (Emphasis added.)

Applicant submits that the cited references fail to teach or suggest all of the recitations of claim 7. The Witek, Kato, Davari, and Igel references all fail to teach or suggest, for example, that the "semiconductor layer includes an element isolation region which has a connection hole," or "a contact layer provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer," as required by claim 7. Applicant therefore respectfully submits that claim 7 is patentable over the cited references for at least the foregoing reasons. Applicant further submits that claims 8-13 are patentable at least by virtue of their dependency from claim 7.

Claims 14-19

Claims 14-19 were rejected under 35 U.S.C. 102(b) as being anticipated by Witek.

Claim 14

Applicant respectfully submits that Witek fails to teach or suggest recitations of claim 14, such as, "a semiconductor layer provided above the insulation layer, the semiconductor layer having a second electrode provided therein." Witek discloses vertical transistors for use in a fast SRAM. As shown in FIG. 32 of Witek, the conductive interconnect 134 is not a "semiconductor layer," as asserted by the Examiner, since a conductor is significantly different than a semiconductor. Moreover, in claim 14 the semiconductor layer and the second electrode are two distinct elements. The Examiner has not shown that Witek discloses "semiconductor layer having a second electrode provided therein," as required by claim 14. Applicant also notes that an "interconnect" is different that an "electrode." Thus, Witek fails to teach or suggest "a semiconductor layer provided above the insulation layer, the semiconductor layer having a second electrode provided therein", as recited in claim 14.

Consequently, the Witek reference fails to teach or suggest at least each of the above recitations of claim 14. Accordingly, Applicant submits that claim 14 is patentable over the cited reference, and therefore the rejection of claim 14 should be withdrawn. Claims 15-19 would also be patentable at least by virtue of their dependency from claim 14. In the event the Examiner seeks to maintain this ground of rejection, then Applicant respectfully requests that the Examiner cite specific portions of Witek that teach or suggest each of the above-underlined recitations of claim 14.

Claim 16

Claim 16 depends from claim 14, and is therefore patentable at least by virtue of its dependency from claim 14. In addition, Applicant respectfully submits that the Witek fails to teach or suggest numerous recitations of claim 16.

For example, Applicant respectfully submits that Witek fails to teach or suggest that "the second electrode is formed from a second impurity layer", as recited in claim 16. FIG. 32 of Witek clearly shows that the interconnect 134 is a conductor. Moreover, as discussed at col. 10, lines 30-35, "a conductive layer is deposited and patterned to form a conductive interconnect 134." Therefore the conductive interconnect 134 is not "formed from a second impurity layer," as required by claim 16. Thus, Witek also fails to teach or suggest that "the second electrode is formed from a second impurity layer", as recited in claim 16.

Accordingly, the Witek reference fails to teach or suggest at least each of the above recitations of claim 16, and the rejection of claim 16 based on Witek should also be withdrawn.

Claim 17

Claim 17 depends from claim 14, and is therefore patentable at least by virtue of its dependency from claim 14. In addition, Applicant respectfully submits that the Witek fails to teach or suggest numerous recitations of claim 17.

For example, Applicant respectfully submits that Witek fails to teach or suggest "a conductive layer provided above the semiconductor layer or in the semiconductor layer", as recited in claim 17. As noted above, Witek fails to teach or suggest the claimed semiconductor layer. Therefore, the conductive layer 140 is not "a conductive layer provided above the semiconductor layer or in the semiconductor layer", as recited in claim 17. Thus, Witek also fails to teach or suggest that "a conductive layer provided above the semiconductor layer or in the semiconductor layer", as recited in claim 17.

Accordingly, the Witek reference fails to teach or suggest at least each of the above recitations of claim 17, and the rejection of claim 17 based on Witek should also be withdrawn.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: March 7, 2003

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Version with markings to show changes made:

IN THE CLAIMS:

Please amend claims 1, 5 and 7 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a first conductive layer provided therein;

an insulation layer provided above the semiconductor substrate;

a semiconductor layer provided above the insulation layer, wherein the semiconductor layer includes an element isolation region which has a connection hole; [and]

a second conductive layer provided above the semiconductor layer or in the semiconductor layer, and electrically connected to the first conductive layer; and

a contact layer provided in the connection hole, the contact layer electrically connecting the first conductive layer and the second conductive layer.

5. (Amended) The semiconductor device as defined by claim 1,

wherein a connection hole is provided for connecting the first conductive layer to the second conductive layer, and

wherein the connection hole extends into the semiconductor substrate, and

wherein a contact layer is provided in the connection hole.

7. (Amended) A semiconductor device comprising:

a semiconductor substrate having a contact region provided therein;

an insulation layer provided above the semiconductor substrate; and

a semiconductor layer provided above the insulation layer, wherein the semiconductor layer includes an element isolation region which has a connection hole; [and]

a conductive layer provided above the semiconductor layer or in the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, [said] the contact region being electrically connected to [said] the conductive layer; and

a contact layer provided in the connection hole, the contact layer electrically connecting the contact region and the conductive layer.